2005 IRPS SUBMISSION COVER PAGE

Paper Title: Methodology For Assessing IC Electromigration-Based Wearout Lifetime Using Stressed SEM/EBSD/OIM

Author's Names: Gary Gaugler, Ph.D., Microtechnics, Inc.

Primary Contact:
Name: Gary Gaugler, Ph.D.
Address: 7970 Twin Rocks Rd
Granite Bay, CA 95746 USA
Telephone: 916-791-8191
Fax: 916-791-8186
Email: gary@microtechnics.com

Secondary Contact:
Name:
Address:

Telephone:
Fax:
Email:

50 WORD ABSTRACT: This IC evaluation work is directed towards providing a quantitative method of predicting the lifetime of COTS ICs when used in other than commercial applications--especially when used in military applications. Of the numerous IC failure mechanisms, this work focuses on electromigration and metal interconnect degradation via analysis with electron backscatter diffraction (EBSD) in the scanning electron microscope (SEM). Through the use of EBSD analysis, long term high temperature exposure and a constant flow of current, effects of accelerated stressing of interconnects can be measured and quantified and may form a novel basis for lifetime prediction.

Suggested Area: Interconnects

Please place an "X" in the boxes of your choice:

Submission Type: ☒ Platform presentation preferred; or ☐ Poster only

Manuscript Status: ☐ Camera-ready submission* or ☒ Two page summary now/full paper upon acceptance

**Camera-ready poster submissions cannot exceed 2 pages. Camera-ready platform presentations submissions are unlimited in length.*

Publicity Release: As the contact submitting the above paper/poster submission, I understand that information from the submission including the graphics/figures may be used as part of the pre-symposium publicity by the IRPS Publicity Committee. IRPS may request publication artwork from me to enhance the promotion of my material. In addition I or one of my co-authors may be requested to meet with the press while attending IRPS.

An "X" in one of the boxes below signifies that I/we do not object to this arrangement or I/we do object to this arrangement. Please place an "X" in the appropriate box below.

☒ **Do Not Object** ☐ **Object**

Submit this page with your paper/poster to TECHNICAL.CHAIR@IRPS.ORG

METHODOLOGY FOR ASSESSING IC ELECTROMIGRATION-BASED WEAROUT LIFETIME USING STRESSED SEM/EBSD/OIM

Gary Gaugler, Ph.D.
Microtechnics, Inc.
7970 Twin Rocks Rd. Granite Bay, CA 957461
916-791-8191; fax:916-791-8186; e-mail: gary@microtechnics.com

PURPOSE

This IC evaluation work aims to provide a quantitative method of predicting the lifetime of COTS ICs when used in other than commercial applications--especially when used in military applications. Of the numerous IC failure mechanisms, this work focuses on electromigration and metal interconnect degradation via analysis with electron backscatter diffraction (EBSD) in the scanning electron microscope (SEM). Through the use of EBSD analysis, long term high temperature exposure, and a constant flow of current, effects of accelerated stressing of interconnects can be measured and quantified and may form a novel basis for lifetime prediction.

[*Keywords*: COTS ICs, integrated circuits, microelectronics, EBSD, wearout, lifetime prediction.]

PROBLEM STATEMENT

Much has been researched and written about the physics of failure of integrated circuits. This topic has become especially more important as devices move to extreme sub-micron dimensions. When using commercial off-the-shelf (COTS) ICs, there is very little information available to the system designer about the inherent reliability or probability of early wearout of components being selected. When applied in a harsh or military environment, the problem becomes even more onerous. Consequently, a method of assessing the inherent wearout lifetime of COTS ICs would benefit system designers when initially selecting components for use in environmentally challenging systems. Of the numerous wearout physics of failure mechanisms such as gate oxide breakdown, hot carrier damage, package composition, etc., resistance to electromigration stands out as a potential key indicator of long term reliability. The challenge is to establish a repeatable method of quantifying the susceptibility of COTS ICs to early wearout based on susceptibility to electromigration.

DISCUSSION

EBSD has been shown to be effective in analyzing Copper interconnects.[1] Furthermore, these researchers stated that “Cu microstructures vary dramatically as a function of processing conditions, including electroplating bath chemistry, sub-layer material, stacking sequence of sub-layers, annealing conditions, and line widths and depths.” These authors performed EBSD on electroplated specimens rather than on manufactured IC interconnects. A typical copper damascene process begins with a thin PVD Ta barrier layer followed by a thin PVD copper seed layer and finally, an electroplated copper fill. Given the complexities of this fabrication process, and the number of variables associated with the resulting copper, using EBSD on actual interconnects for the measurement of grain structure, boundary, phase and twins analysis is considered to be a potentially powerful tool for evaluating the long term viability of commercial microcircuits. The problem at hand is one of developing a method for performing EBSD on specific COTS ICs rather than on interconnect materials in general.

Metal interconnects conduct current either continuously, or in an on and off manner. Supply voltage interconnects conduct a continuous average value of current, while circuit interconnects vary in switching demands--number of switchings per second, duty cycle and amount of current. The flow of current through a conductor can cause electromigration. This is the transport of metal ions through a conductor. Rather than a normal random diffusion process, current conduction causes a directional diffusion process caused by charge carriers.[2] Normally, electromigration is associated with conduction of direct current. In a microcircuit, there are portions which are essentially steady state, such as the power supply connections. However, the majority of interconnections carry time varying signals which are thus not steady state. If one considers current density of conductors, then conductors which carry switched signals may integrate over time to the point where small sized conductors exhibit similar effects as do steady state conductors. This could be particularly true for interconnects where the height-to-width ratio of the conductor is greater than one, as this can lead to the formation of twins.

This new work is the development of a repeatable method of exposing the COTS IC interconnects for subsequent EBSD analysis. Figure 1 shows a typical damascene device with the top level exposed. Underneath this level are wide interconnects as well as progressively narrower interconnects.

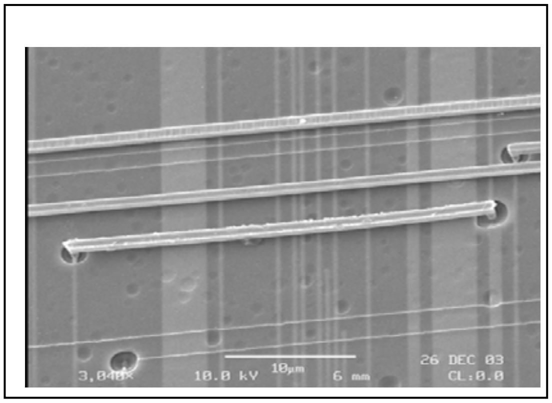

FIGURE 1. EXPOSED TOP LEVEL

Using 50:1 BOE wet etching, subsequent layers can be exposed. Additional etching exposes the upper and lower layers of metal interconnects. This is a delicate operation to perform but provides exceptional benefits for ultimately making electrical contact away from the main interconnect. It further delineates the vertical interconnect such that current flow effects may be more readily observed at this area.

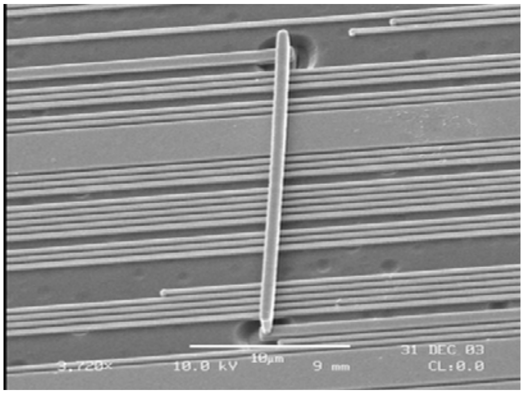

FIGURE 2. AFTER REMOVAL OF ADDITIONAL INTERLAYER DIELECTRIC

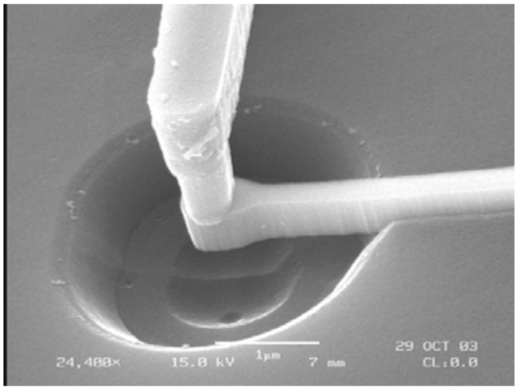

FIGURE 3. DETAIL OF VIA AND INTERCONNECT FROM ONE LEVEL TO ANOTHER

Figures 2 and 3 show how subsequent etching can further expose the interconnects. Of note in Figure 3 is that the lower level interconnect is still mechanically retained in the interlayer dielectric. This is highly desirable as to ensure that the lower level interconnect remains as rigid as possible during thermal stressing.

Figure 4 shows the proposed FIB cutting of lower level metal to allow on-center probe contact of the small interconnects.

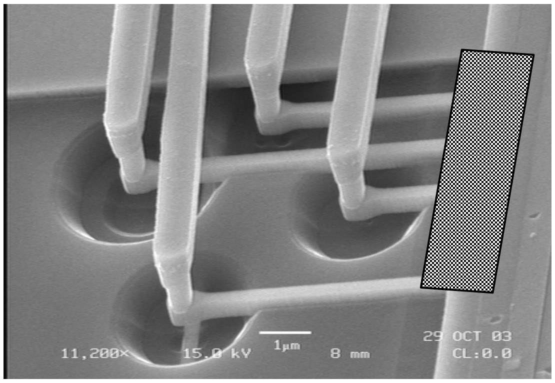

FIGURE 4. FIB CUT TO EXPOSE ONE SET OF ENDS OF RUNNERS

Once both ends of one or more runners are exposed and isolated, pre-stress baseline EBSD is performed. The sequence of pre-stress analysis forms a baseline of grain structure, phase and orientation of the interconnect as-is. One or more of the interconnects are analyzed using EBSD at room temperature and then at elevated temperature and with constant current flowing in the interconnect. Two Omniprobe 100.5 nano probes are used to position Tungsten tips at the center of each end of a runner and allow for current to be passed through the interconnect. This is performed in the SEM while the IC specimen is heated to and maintained at 150F for three weeks. After this time, the stressed interconnect is analyzed again with EBSD under the same conditions, and the results are compared to the baseline data.

The EBSD Orientation Imaging Map (OIM) analysis shows the before and after stressing of interconnect grain size distribution, misorientation, twins formation and crystal orientation distribution. As runner width is reduced, grain size tends to converge on the metal runner width at 0.2um.[1] Consequently, long but narrow grains could have vulnerabilities to environmental changes and to the formation of twins.

EXPERIMENTAL SETUP

The equipment complement to perform stressed EBSD analysis in the SEM is a critical element of this reliability assessment methodology. The fundamental tool is the SEM. The SEM used for this work is a Zeiss Supra 55VP with three EDS ports and high probe current option (20nA). The usefulness of Variable Pressure (VP) mode is to enable high resolution imaging of the de-passivated, exposed microcircuit specimen while avoiding charging. The specimen is positioned at zero degrees tilt and moved in the X and Y directions until a candidate interconnect is centered in the image at an associated magnification. Then, image shift is used to center the image on one side of the interconnect for placement of the nano probe in the center end of that interconnect. The image is then shifted to the other end of the interconnect and the second nano probe is placed on the center of that interconnect. The Omniprobe 100.5 nano probes readily accommodate positioning of their Tungsten probe tips at the center of 0.2um wide interconnects or smaller while also providing electrical contact.

The specimen and probes are then in position to allow the conduction of current through the selected interconnect. The specimen is mounted using conductive epoxy onto an Aluminum specimen holder which is part of a Deben XP extended temperature range thermal controlled stage mount. The XP is used to set the specimen temperature to the selected temperature (150C in this case). The effects of varying the specimen temperature can be observed over separate experimental runs.

EBSD is initially performed on the specimen before it has been thermally or temperature stressed. This is accomplished with an EDAX/TSL OIM EBSD system. The specimen is tilted to seventy degrees and one nano probe is used with the SEM in VP mode (~25 Pa) to contact one end of the selected interconnect to ground it--grounding the interconnect eliminates charging. The SEM is then operated in higher vacuum mode and the accelerating potential is increased from approximately 3KV to 20KV to support generation of Kikuchi patterns for EBSD. The specimen is then placed at zero tilt, stressed and re-positioned to seventy degrees tilt for after-stress EBSD. One nano probe is again used to prevent charging.

The ability to image, probe and conduct current through the isolated interconnect is tightly based on the combination of variable pressure SEM imaging and contact to ground using the nano probe. If the specimen were coated to reduce charging, Kikuchi pattern quality would be greatly reduced. Quality can be reduced to the point that data collection is not possible. Another factor in this methodology is that the interconnects are not polished. Traditional EBSD specimens are highly polished and are conductive. By using the nano probe to ground the interconnect, charging is eliminated. Adjusting SEM KV and chamber vacuum allows for optimization of Kikuchi pattern quality.

REFERENCES

[1] D. Field, T. Muppidi & J. Sanchez, “Electron Backscatter Diffraction Characterization of Inlaid Cu Lines for Interconnect Applications,” in Scanning, November/December 2003. pp. 309-315.

[2] N. Weste & K. Eshraghian, 1993. *Principles of CMOS VLSI Design*. Addison-Wesley Publishing Company, 1993, pg. 238.